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EXAMINER	
LEE, CHRISTOPHER E	

ART UNIT	PAPER NUMBER
2112	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/070,991	DIEHL, MICHAEL	
	Examiner	Art Unit	
	Christopher E. Lee	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 March 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *22-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *22-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 March 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/14/02 3/24/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the Preliminary Amendment filed on 14th of March 2002. No claim has been amended; claims 1-21 have been canceled; and claims 22-42 have been newly added. Currently, claims 22-42 are pending in this application.

Claim Objections

2. Claims 23-29, 31-36 and 38-42 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. The claims' dependency numberings are incorrect. The Examiner assumes their correct dependencies in light of the specification for the purpose of the claim rejection based on prior art.

3. Claim 28 is objected to because of the following informalities: delete "comprise" in line 2. Appropriate correction is required.

Drawings

4. Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated on page 2, lines 4-11 in the Application. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 22-42 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claims 22 and 30 recite the limitation "the status of the output area and of the input area" in line 9 of the claim 22, and in line 7 of the claim 30, respectively.

There is insufficient antecedent basis for this limitation in the claim. Therefore, the term "the status of the output area and of the input area" could be considered as --a status of the output area and of the input area-- since it is not clearly defined in the claims.

The claim 27 recites the limitation "the input area of the active component" in lines 2-3. There is insufficient antecedent basis for this limitation in the claim. Actually, the subject matter "input area" is defined in line 6-7 of the claim 22 as the input area to store data read in via the serial interface and to be read out via the bus interface within the passive component. Therefore, the term "the input are of the active component" could be considered as --a corresponding input area of the active component-- since it is not clearly defined in the claims.

The claims 23-29 are dependent claims of the claim 29.

The claim 30 recites the limitation "the output area of the passive component" in lines 3-4, "the input area of the passive component" in line 5, and "the passive element" in line 9. There is insufficient antecedent basis for these limitations in the claim. Therefore, the term "the output area of the passive component" could be considered as --an output area of the passive component--, the term "the input area of the passive component" could be considered as --an input area of the passive component--, and the term "the passive element" could be considered as --the passive component-- since those are not clearly defined in the claims.

The claims 31-36 are dependent claims of the claim 30.

The claim 37 recites the limitation "the request of the active component" in line 6, and "the status of the output areas and of the input areas" in line 7. There is insufficient antecedent basis for these limitations in the claim. Therefore, the term "the request of the active component" could be considered as --a request of the active component--, and the term "the status of the output areas and of the input areas" could be considered as --a status of the output areas and of the input areas-- since those are not clearly defined in the claims.

The claims 38-42 are dependent claims of the claim 30.

The claim 41 recites the limitation "the read-out data packets" in line 1, and "the read-in data packets" in lines 1-2. There is insufficient antecedent basis for these limitations in the claim. Therefore, the term "the read-out data packets" could be considered as --read-out data packets--, and the term "the read-in data packets" could be considered as --read-in data packets-- since those are not clearly defined in the claims.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 22, 28-30, 32, 35 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamada et al. [US 4,745,540; cited by the Applicant; hereinafter Hamada] in view of Thomsen et al. [US 5,278,956; hereinafter Thomsen].

Referring to claim 22, Hamada discloses a passive component (i.e., I/O and Signal Converting Units in Fig. 2) for a bus system (i.e., Process Input/Output System; See col. 1,lines 5-11), comprising: a bus interface (i.e., Bus Noise Eliminating Portion 62 and Bus Control Portion 60 in Fig. 2) to connect to a bus (i.e., Bus 150 of Fig. 2); a serial interface (i.e., Signal Converting Units 40 and 50 in Fig. 2), to

serially read out (i.e., SO in Fig. 2) and read in (i.e., SI in Fig. 2) data (See col. 3, line 48 through col. 4, line 21); a data memory (i.e., Data Storage Portions 47 and 57 in Fig. 2) with an output area (i.e., Data Storage Portion 57 of Fig. 2) to store data read in via said bus interface and to be read out via said serial interface (See col. 4, lines 12-15); an input area (i.e., Data Storage Portion 47 of Fig. 2) to store data read in via said serial interface and to be read out via said bus interface (See col. 3, lines 65-68); a control device (i.e., Input Control Portion 41 and Output Control Portion 51 in Fig. 2) to control said transmission and storage of data (See col. 3, lines 58-64 and col. 4, lines 5-11).

Hamada does not expressly teach a detection device to detect a status of said output area and of said input area and provide corresponding status information, which status information is used as the basis for reading data into said output area and reading data out of said input area via said bus interface when said bus system is connected.

Thomsen discloses a variable size FIFO memory (See Fig. 1 and col. 2, lines 48-65), wherein a detection device (i.e., READ ADDR COUNTER 100, WRITE ADDR COUNTER 102, and WRITE MINUS READ 104 in Fig. 1) to detect a status (i.e., status of data level in FIFO; See col. 3, lines 17-21) of an output area (i.e., TRANSMITTER FIFO 18 of Fig. 4B) and of an input area (i.e., RECEIVER FIFO 12 of Fig. 4B) and provide corresponding status information (i.e., Amount of Data Available in Fig. 1), which status information is used as the basis for reading data into said output area and reading data out of said input area (See col. 3, lines 24-31) via a bus interface (i.e., FIFO access via internal data bus and its interface in Fig. 4A) when a bus system (i.e., data processing system 15 of Fig. 4A) is connected (See col. 6, lines 3-19).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted said data memory, as disclosed by Hamada, by said variable size FIFO memory, as disclosed by Thomsen, for the advantage of providing a data available interrupt circuit with a variable threshold for reading data from said input area (i.e., receiver FIFO), and a variable depth data memory

(i.e., FIFO) where the depth of said data memory (i.e., FIFO) is selectable for use as either said output area (i.e., receiver FIFO) or said input area (i.e., transmitter FIFO) of said serial interface (i.e., UART; See Thomsen, col. 1, lines 60-65).

Referring to claim 28, Thomsen teaches said detection device (i.e., READ ADDR COUNTER 100, WRITE ADDR COUNTER 102, and WRITE MINUS READ 104 in Fig. 1) comprises an acknowledgement counter (i.e., WRITE ADDR COUNTER 102 of Fig. 1) to count data packets which are read out via said serial interface (i.e., writing out Transmitter FIFO 18 for SOUT in Fig. 4B), and a sequence counter (i.e., READ ADDR COUNTER 100 of Fig. 1) to count data packets which are read in via said serial interface (i.e., reading in Receiver FIFO 12 via SIN in Fig. 4B), said counting values serving as said status information (i.e., amount of data available; See col. 3, lines 10-23).

Referring to claim 29, Thomsen teaches a maximum size of said input area and of said output area can be set in a variable fashion (i.e., selecting the depth of a variable depth FIFO; See Abstract and col. 1, lines 60-68), said data packets which are to be stored therein being able to have any desired sizes within said respectively set maximum size (See col. 3, line 56 through col. 4, line 21).

Referring to claim 30, Hamada discloses an active component (i.e., I/O and Signal Converting Units in Fig. 2) for exchanging data with a passive component (i.e., exchanging data among External Units on Process Input/Output System in Fig. 1; See col. 1,lines 5-11), comprising: a bus interface (i.e., Bus Noise Eliminating Portion 62 and Bus Control Portion 60 in Fig. 2) to connect to a bus (i.e., Bus 150 of Fig. 2); a data memory (i.e., Data Storage Portions 47 and 57 in Fig. 2) with an output area (i.e., Data Storage Portion 57 of Fig. 2) to store data in an output area of said passive component (i.e., data memory for transmitting data of External Unit on Bus 150 in Fig. 2; See col. 4, lines 48-62) and to be read out via a serial interface (i.e., Signal Converting Units 40 and 50 in Fig. 2; See col. 4, lines 12-15); an input area (i.e., Data Storage Portion 47 of Fig. 2) of data which is read out of an input area of said passive component (i.e., data memory for receiving data from SI to External Unit on Bus 150 in Fig. 2; See col.

3, lines 65-68); (i.e., Input Control Portion 41 and Output Control Portion 51 in Fig. 2) to control said transmission and storage of data (See col. 3, lines 58-64 and col. 4, lines 5-11).

Hamada does not expressly teach a detection device to detect a status of said output area and of said input area and provide status information, which status information is used by said active component, as the basis for reading data from said passive component into said input area via said bus interface and reading data out of said output area to said passive component.

Thomsen discloses a variable size FIFO memory (See Fig. 1 and col. 2, lines 48-65), wherein a detection device (i.e., READ ADDR COUNTER 100, WRITE ADDR COUNTER 102, and WRITE MINUS READ 104 in Fig. 1) to detect a status (i.e., status of data level in FIFO; See col. 3, lines 17-21) of an output area (i.e., TRANSMITTER FIFO 18 of Fig. 4B) and of an input area (i.e., RECEIVER FIFO 12 of Fig. 4B) and provide status information (i.e., Amount of Data Available in Fig. 1; See col. 3, lines 24-31), which status information is used by an active component (i.e., UART; See col. 6, lines 3-19), as the basis for reading data from a passive component into said input area bus interface (i.e., SIN in Fig. 4B; See col. 6, lines 12-19) and reading data out of said output area to said passive component (i.e., SOUT in Fig. 4B; See col. 6, lines 5-11).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted said data memory, as disclosed by Hamada, by said variable size FIFO memory, as disclosed by Thomsen, for the advantage of providing a data available interrupt circuit with a variable threshold for reading data from said input area (i.e., receiver FIFO), and a variable depth data memory (i.e., FIFO) where the depth of said data memory (i.e., FIFO) is selectable for use as either said output area (i.e., receiver FIFO) or said input area (i.e., transmitter FIFO) of said serial interface (i.e., UART; See Thomsen, col. 1, lines 60-65).

Referring to claim 32, Hamada teaches a serial interface (i.e., SI and SO in Fig. 2) to serially read data into said output area (i.e., serial data input via SI into Data Storage Portion 47 in Fig. 2; See col. 3,

lines 52-54) and to serially read data out of said input area (i.e., serial data output via SO from Data Storage Portion 57 in Fig. 2; See col. 4, lines 15-19).

Referring to claim 35, Thomsen teaches said detection device (i.e., READ ADDR COUNTER 100, WRITE ADDR COUNTER 102, and WRITE MINUS READ 104 in Fig. 1) comprises an acknowledgement counter (i.e., WRITE ADDR COUNTER 102 of Fig. 1) to count data packets which are read out via said serial interface (i.e., writing out Transmitter FIFO 18 for SOUT in Fig. 4B), and a sequence counter (i.e., READ ADDR COUNTER 100 of Fig. 1) to count data packets which are read in via said serial interface (i.e., reading in Receiver FIFO 12 via SIN in Fig. 4B), said counting values serving as said status information (i.e., amount of data available; See col. 3, lines 10-23).

Referring to claim 36, Thomsen teaches a maximum size of said input area and of said output area can be set in a variable fashion (i.e., selecting the depth of a variable depth FIFO; See Abstract and col. 1, lines 60-68), said data packets which are to be stored therein being able to have any desired sizes within said respectively set maximum size (See col. 3, line 56 through col. 4, line 21).

9. Claims 33 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamada [US 4,745,540] in view of Thomsen [US 5,278,956] as applied to claims 22, 28-30, 32, 35 and 36 above, and further in view of Feder [US 5,872,845 A].

Referring to claim 33, Hamada, as modified by Thomsen, discloses all the limitations of the claim 33 except that does not expressly teach a data packet is not read into said output area of said active component via said serial interface until said output area of said passive component is ready to receive said data packet.

Feder discloses a method and apparatus for interfacing FAX machines to digital communication networks (See Abstract and Fig. 1), wherein a data packet (i.e., packets on digital communication networks) is not read into an output area of an active component (i.e., Server 130 of Fig. 1) via an serial interface (i.e.,

digital communication networks) until an output area of a passive component (i.e., interface 160 of Fig. 1) is ready to receive said data packet (See col. 6, line 65 through col. 7, line 9).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said method of handshaking, as disclosed by Feder, in said data transferring, as disclosed by Hamada, as modified by Thomsen, so as to prevent said output area (i.e., memory) overflow in said passive component (i.e., interface; See Feder, col. 6, lines 65-67).

Referring to claim 34, Hamada, as modified by Thomsen, discloses all the limitations of the claim 34 except that does not expressly teach a data packet to be read out via said serial interface is not read from said input area of said passive component into said input area of said active component until said input area of said active component is ready to receive said data packet.

Feder discloses a method and apparatus for interfacing FAX machines to digital communication networks (See Abstract and Fig. 1), wherein a data packet (i.e., packets on digital communication networks) to be read out via a serial interface (i.e., interface to FAX 170 in Fig. 1) is not read from an input area of a passive component (i.e., Server 130 of Fig. 1) into an input area of an active component (i.e., interface 160 of Fig. 1) until said input area of said active component (i.e., interface) is ready to receive said data packet (See col. 6, line 65 through col. 7, line 9).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said method of handshaking, as disclosed by Feder, in said data transferring, as disclosed by Hamada, as modified by Thomsen, so as to prevent said output area (i.e., memory) overflow in said passive component (i.e., interface; See Feder, col. 6, lines 65-67).

10. Claim 37 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tretter et al. [US 5,927,218 A; cited by the Applicant; hereinafter Tretter] in view of Thomsen [US 5,278,956].

Referring to claim 37, Tretter discloses a method for reading serial data into and out of a bus system (See col. 1, lines 38-43) which comprises a passive component (i.e., ASIC 4 of Fig. 2), forming a

slave station (i.e., decentralized peripheral module 3 in Fig. 1; See col. 1, lines 60-61), with a serial interface (i.e., bus interface 17 of Fig. 2) and a data memory (i.e., storages 10 and 11in Fig. 2), which has an output area (i.e., input signal storage 10 in Fig. 2) for reading out data via said serial interface (i.e., bus interface; See col. 2, lines 16-22) and comprises an input area (i.e., output storage 11 in Fig. 2; See col. 2, lines 22-27), and an active component (i.e., CPU 1 of Fig. 1), forming a master station (i.e., stored program controller; See col. 1, lines 59-60), with a data memory which has an output area and an input area (i.e., means for storing input/output signals in CPU 1 of Fig. 1; See col. 2, lines 20-23), comprising: transferring data at a request of said active component (i.e., at a control by stored-program controller CPU 1 of Fig. 1) via said passive component (See col. 2, lines 16-27).

Tretter does not expressly teach a method step of detecting a status of said output areas and of said input areas and providing status information corresponding to said status, which status information is used as the basis for said transfer of said data of said output area of said active component into said output area of said passive component, and said transfer of said data of said input area of said passive component into said input area of said active component.

Thomsen discloses a variable size FIFO memory (See Fig. 1 and col. 2, lines 48-65), wherein detecting a status (i.e., status of data level in FIFO; See col. 3, lines 17-21) of an output areas (i.e., TRANSMITTER FIFO 18 of Fig. 4B) and of an input areas (i.e., RECEIVER FIFO 12 of Fig. 4B) and providing status information corresponding to said status (i.e., Amount of Data Available in Fig. 1; See col. 3, lines 24-31), which status information is used as the basis for transfer of data of said output area of an active component (i.e., UART; See col. 6, lines 3-19) into said output area of a passive component (i.e., SOUT to memory of communication station 17 in Fig. 4B; See col. 6, lines 5-11), and said transfer of said data of said input area of said passive component (i.e., from memory of communication station 17 of Fig. 4B) into said input area of said active component (i.e., SIN into memory of UART in Fig. 4B; See col. 6, lines 12-19).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted said data memory, as disclosed by Tretter, by said variable size FIFO memory, as disclosed by Thomsen, for the advantage of providing a data available interrupt circuit with a variable threshold for reading data from said input area (i.e., receiver FIFO), and a variable depth data memory (i.e., FIFO) where the depth of said data memory (i.e., FIFO) is selectable for use as either said output area (i.e., receiver FIFO) or said input area (i.e., transmitter FIFO) of said serial interface (i.e., UART; See Thomsen, col. 1, lines 60-65).

11. Claims 39-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tretter [US 5,927,218 A] in view of Thomsen [US 5,278,956] as applied to claim 37 above, and further in view of Feder [US 5,872,845 A].

Referring to claim 39, Tretter, as modified by Thomsen, discloses all the limitations of the claim 39 except that does not expressly teach a data packet is not read into said output area of said active component until said output area of said passive component is ready to receive said data packet.

Feder discloses a method and apparatus for interfacing FAX machines to digital communication networks (See Abstract and Fig. 1), wherein a data packet (i.e., packets on digital communication networks) is not read into an output area of an active component (i.e., Server 130 of Fig. 1) until an output area of a passive component (i.e., interface 160 of Fig. 1) is ready to receive said data packet (See col. 6, line 65 through col. 7, line 9).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said method of handshaking, as disclosed by Feder, in said data transferring, as disclosed by Tretter, as modified by Thomsen, so as to prevent said output area (i.e., memory) overflow in said passive component (i.e., interface; See Feder, col. 6, lines 65-67).

Referring to claim 40, Tretter, as modified by Thomsen, discloses all the limitations of the claim 40 except that does not expressly teach a data packet is not read from said input area of said passive

component into said input area of said active component until said input area of said active component is ready to receive said data packet.

Feder discloses a method and apparatus for interfacing FAX machines to digital communication networks (See Abstract and Fig. 1), wherein a data packet (i.e., packets on digital communication networks) is not read from an input area of a passive component (i.e., Server 130 of Fig. 1) into an input area of an active component (i.e., interface 160 of Fig. 1) until said input area of said active component (i.e., interface) is ready to receive said data packet (See col. 6, line 65 through col. 7, line 9).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said method of handshaking, as disclosed by Feder, in said data transferring, as disclosed by Tretter, as modified by Thomsen, so as to prevent said output area (i.e., memory) overflow in said passive component (i.e., interface; See Feder, col. 6, lines 65-67).

Referring to claim 41, Thomsen teaches read-out data packets (i.e., WRITE ADDR COUNTER 102 of Fig. 1 to count data packets writing out Transmitter FIFO 18 for SOUT in Fig. 4B) and read-in data packets (i.e., READ ADDR COUNTER 100 of Fig. 1 to count data packets reading in Receiver FIFO 12 via SIN in Fig. 4B) are counted, said counting values serving as said status information (i.e., amount of data available; See col. 3, lines 10-23).

Referring to claim 42, Thomsen teaches a maximum size of said input area and of said output area can be set in a variable fashion (i.e., selecting the depth of a variable depth FIFO; See Abstract and col. 1, lines 60-68), said data packets to be stored therein being able to have any desired sizes within said respectively set maximum size (See col. 3, line 56 through col. 4, line 21).

Allowable Subject Matter

12. Claims 23-27, 31 and 38 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

13. The following is a statement of reasons for the indication of allowable subject matter:

The limitations of claim 23 are deemed allowable over the prior art of record as the prior art fails to teach or suggest that a comparative device in said passive component periodically compares said status information with corresponding status information of an active component of a connected bus system. The claims 24-27 are the dependent claims of the claim 23.

The limitations of claim 31 are deemed allowable over the prior art of record as the prior art fails to teach or suggest that a comparative device in said active component periodically compares said status information with corresponding status information of said passive component.

The limitations of claim 38 are deemed allowable over the prior art of record as the prior art fails to teach or suggest that a method step of comparing the status information of the output areas of the active and passive components and periodically comparing the status information of the input areas of the active and passive components, and reconciliation of the output areas and the input areas carried out on the basis of comparison.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

With regard to Process Control,

Schrier et al. [US 6,055,633 A] disclose method of reprogramming memories in field devices over a multidrop network.

Brown et al. [US 6,192,281 B1] disclose network accessible interface for a process control network.

Eryurek [US 6,370,448 B1] disclose communication technique for field devices in industrial processes.

With regard to Serial-Parallel Bus interfacing,

Mullins et al. [US 5,596,724 A] disclose input/output data port with a parallel and serial interface.

Grote et al. [US 4,728,930] disclose parallel-to-serial data interface adapter.

Kobayashi [US 6,611,557 B1] discloses serial data receiver.

With regard to Data Transferring System,

Buhler et al. [US 6,192,036 B1] disclose method of operating a data transmission system.

Nakamura et al. [US 5,832,308 A] disclose apparatus for controlling data transfer between external interfaces through buffer memory using a FIFO, an empty signal, and a full signal.

Yanbe [US 6,510,449 B1] discloses data transmission system.

Dolkas et al. [US 5,007,051] disclose link layer protocol and apparatus for data communication.

Fesas, Jr. [US 6,397,316 B2] disclose system for reducing bus overhead for communication with a network interface.

With regard to Data Buffering for Data Communication,

Kobunaya [US 5,663,948 A] discloses communication data receiver capable of minimizing the discarding of received data during an overflow.

Bradley et al. [US 5,430,847 A] disclose method and system for extending system buses to external devices.

Ugajin et al. [US 5,046,039] disclose buffer management system.

Rickard et al. [US 6,041,397 A] disclose efficient transmission buffer management system.

Banman et al. [US 5,557,751 A] disclose method and apparatus for serial data communication using FIFO buffers.

With regard to Master-Slave Bus system,

Jasperneite et al. [US 6,421,710 B1] disclose complying arrangement for a master-slave bus system.

Tezuka et al. [US 5,132,680 A] disclose polling communication system with priority control.

DiGiulio et al. [EP 0 503 323 A2] disclose serial bus interface and method.

Ihara et al. [JP 408044661 A] disclose information processor.

15. The Examiner refers to Ihara [JP 408044661 A] reference as a prior art for the claim rejection(s) in the instant Office Action, and it is referred to the original copy of foreign reference in foreign language (i.e., Japanese). The Examiner attaches a machine translated copy of the reference for the convenience of the Applicant. However, the Examiner cautions the Applicant that the Office is not responsible for any erroneous interpretation resulting from inaccuracies between the original foreign language reference and the machine translation of the reference, as the machine translation may not reflect the original precisely.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 703-305-5950. The examiner can normally be reached on 9:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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